

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Publication Number

Publication Number

Applicant(s)

Filing Date

Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SW	A	6,137,130	10/2000	SUNG	257	306	
SW	B	6,136,646	10/2000	LINLIU et al.	438	255	
SW	C	US 2002/0037644A1	03/2002	RHA et al.	438	656	
SW	D	6,180,970 B1	01/2001	HWANG et al.	257	295	
SW	E	6,239,461 B1	05/2001	LEE	257	306	
SW	F	5,296,095	03/1994	NABESHIMA et al.	156	662	
SW	G	5,726,499	03/1998	IRINODA	257	774	
SW	H	6,348,709 B1	02/2002	GRAETTINGER et al.	257	311	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
SW	I	5-13750	01/22/1993	JAPAN				
SW	J	7-297280	11/10/1995	JAPAN				
SW	K	JP407297280A	10/1995	JAPAN				
SW	L	JP2000-040805A	02/2000	JAPAN				
SW	M	2001-0055403	07/04/2001	REPUBLIC OF KOREA				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

SW	N	Miyashita, T. et al., "A Novel Bit-Line Process using Ploy-Si Masked Dual-Damascene (PMDD) for 0.13 microm DRAMs and Beyond", in Electron Devices Mtg, 2000, IEDM Techn. Digest, 12/10/2000-12/13/2000, San Francisco, CA (USA) (INSPEC Accession No: 6880863).

EXAMINER

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DATE CONSIDERED

7/9/04

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